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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **Dabak et al.**
Serial No.: **10/718,338**
Filed: **11/18/2003**

Docket Number: **TI-28984.1**
Art Unit: **2616**
Examiner: **Patel, Chandras B.**
Conf. No.: **9249**

For: **SPACE TIME TRANSMIT DIVERSITY FOR TDD/WCDMA SYSTEMS**

CERTIFICATION OF FACSIMILE TRANSMISSION

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March 5, 2009
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FACSIMILE COVER SHEET

X FACSIMILE COVER SHEET	X APPEAL BRIEF (16 Pages)
___ NEW APPLICATION	___ INTERVIEW SUMMARY (# Pages)
___ DECLARATION (# Pages)	___ NOTICE OF APPEAL (# Page)
___ ASSIGNMENT (# Pages)	___ APPEAL (# Pages)
___ FORMAL DRAWINGS	___ FEE TRANSMITTAL (# Page)
___ INFORMAL DRAWINGS	
___ CONTINUATION APP'N (# Pages)	
___ DIVISIONAL APP'N	

NAME OF INVENTOR(S): *Dabak et al.*	RECEIPT DATE & SERIAL NO.: **10/718,338**
	FILING DATE: ***November 18, 2003***
TITLE OF INVENTION: **SPACE TIME TRANSMIT DIVERSITY FOR TDD/WCDMA SYSTEMS**	
TI FILE NO.: *TI-28984.1* DEPOSIT ACCT. NO.: *20-0668*	
DATE FAXED: ***March 5, 2009*** DUE: ***March 13, 2009*** ATTY/SEC'Y: ***Robert N. Rountree***	

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APPELLANTS' BRIEF

March 5, 2009

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I hereby certify that the above correspondence is being facsimile transmitted to the Patent and Trademark Office on March 5, 2009.

Robert N. Rountree

Robert N. Rountree, Reg. No. 39,347

Dear Sir:

In support of their appeal of the Final Rejection of claims 28, 30-35, 39-42, and 44-49 in the above-referenced application, Appellants respectfully submit herein their brief. In response to the Notification of non-Compliant Appeal Brief mailed February 13, 2009, please replace the Appeal Brief filed January 6, 2009, with the instant amended Appeal Brief.

1. REAL PARTY IN INTEREST

Texas Instruments Incorporated is the real party in interest.

2. RELATED APPEALS AND INTERFERENCES

No other related appeals or interferences are known to Appellants.

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3. STATUS OF CLAIMS

Claims 28, 30-35, 39-42, and 44-49 are in the application and are reproduced in Appendix A to Appellants' Brief filed herewith. Claim 39 is rejected under 35 U.S.C. § 102(e). Claims 28, 30-35, 40-42, and 44-49 are rejected under 35 U.S.C. § 103(a). Claims 1-27, 29, 36-38, and 43 are cancelled. Claims 28, 30-35, 39-42, and 44-49 are on appeal.

4. STATUS OF AMENDMENTS

There are no outstanding amendments.

5. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 28 is directed to an encoder circuit as described at Figure 2, page 6, line 11 through page 7, line 10. The encoder circuit is coupled to receive a plurality of symbols D^1 through D^k. The encoder circuit produces the plurality of symbols (Figure 2, $D^1{}_1$) at a first output terminal (204) and a transform of the plurality of symbols ($D^1{}_2$) at a second output terminal (206) within a time slot (Figure 3, 302). The encoder circuit produces a sequence of predetermined signals (Figure 4, 422) interposed with the plurality of symbols (page 7, lines 15-21). The encoder circuit is coupled to receive a control signal (Figure 1, 108). The encoder circuit produces the plurality of symbols at the first output terminal and the transform of the plurality of symbols at the second output terminal in response to a first value of the control signal. The encoder circuit produces the plurality of symbols at the first output terminal and does not producing the transform of the plurality of symbols at the second output terminal in response to a second value of the control signal (page 5, line 15 through page 6, line 9).

Independent claim 39 is directed to an encoder circuit (Figure 2, page 6, line 11 through page 7, line 10). The encoder circuit is coupled to receive a plurality of symbols (D^1 through D^K). , The encoder circuit produces the plurality of symbols (Figure 2, $D^1{}_1$ and $D^1{}_2$) and a sequence of predetermined signals (Figure 4, 422, page 7, lines 15-21) at a first (Figure 2, 230) and a second

(236) output terminal. The sequence of predetermined signals comprises a code sequence. A first shift of the code sequence corresponds to the first output terminal (Figure 5B, Antenna 1) and a second shift of the code sequence corresponds to the second output terminal (Figure 5B, Antenna 2). The first and second shifts are directed to an embodiment of the present invention for broadcast channel applications as described at page 8, lines 18-22).

Independent claim 40 is directed to an encoder circuit as described at Figure 2, page 6, line 11 through page 7, line 10. The encoder circuit is coupled to receive a plurality of first symbols (D^1) corresponding to a first user. The encoder circuit produces the plurality of first symbols (Figure 2, D^1_1) at a first output terminal (204) and a transform of the plurality of first symbols (D^1_2) at a second output terminal (206) within a time slot (Figure 3, 302). The encoder circuit is coupled to receive a control signal (Figure 1, 108). The encoder circuit produces the plurality of first symbols at the first output terminal and the transform of the plurality of first symbols at the second output terminal in response to a first value of the control signal. The encoder circuit produces the plurality of first symbols at the first output terminal and does not produce the transform of the plurality of first symbols at the second output terminal in response to a second value of the control signal (page 5, line 15 through page 6, line 9). The encoder circuit includes a first multiplier circuit (208) coupled to receive the plurality of first symbols and arranged to multiply the plurality of first symbols by a code (C^1) corresponding to the first user to produce a first coded signal, wherein the first coded signal is applied to a first antenna (230). The encoder circuit further includes a second multiplier circuit (214) coupled to receive the transform of the plurality of first symbols and arranged to multiply the transform of the plurality of first symbols by the code (C^1) corresponding to the first user to produce a second coded signal, wherein the second coded signal is applied to a second antenna (236).

6. GROUNDS FOR REJECTION TO BE REVIEWED ON APPEAL

A. Claim 39 is rejected under 35 U.S.C. § 102(e) as being anticipated by Whinnett et al. (U.S. Pat. No. 6,317,411).

B. Claims 28, 30-31, 35, 40-41, 44-45, and 49 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Whinnett et al. (U.S. Pat. No. 6,317,411) in view of Secord et al. (U.S. Pat. No. 6,373,831).

7. ARGUMENT

A. Claim 39 is rejected under 35 U.S.C. § 102(e) as being anticipated by Whinnett et al. (U.S. Pat. No. 6,317,411). Claim 39 recites "A circuit, comprising an encoder circuit coupled to receive a plurality of symbols, the encoder circuit producing the plurality of symbols and a sequence of predetermined signals at a first and a second output terminal, wherein the sequence of predetermined signals comprises a code sequence, and wherein **a first shift of the code sequence corresponds to the first output terminal and a second shift of the code sequence corresponds to the second output terminal.**" (emphasis added). The sequence of predetermined signals comprises a code sequence. A first shift of the code sequence corresponds to the first output terminal (Figure 5B, Antenna 1) and a second shift of the code sequence corresponds to the second output terminal (Figure 5B, Antenna 2). The first and second shifts are directed to an embodiment of the present invention for broadcast channel applications as described at page 8, lines 18-22).

As best Appellants now understand the present rejection, Examiner interprets the output of transformer 88 (Figure 5) of Whinnett et al. as first and second shifts of the code sequence of claim 39. This is incorrect for several reasons. First, claim 39 recites a single code sequence. One part of the code sequence (first shift) corresponds to a first output terminal. Another part of the code sequence (second shift) corresponds to a second output terminal. Both are parts of the same code sequence. In an Advisory Action of August 28, 2008, Examiner states "S1S2 from 88 is outputed [sic] as two code sequences as shown in Figure 5." If they are two code sequences, they cannot be two shifts of one code sequence as required by claim 39.

Second, it is not entirely clear whether Examiner interprets the symbols ($S_1S_1S_2S_2$ and $-S_2^*-S_2^*S_1^*S_1^*$), the code of the symbols, or the encoded symbols as "two code sequences." According to Whinnett et al, the symbols are really symbols and not a code sequence. Moreover, the symbols

do not meet the limitations of claim 39 since symbols $S_1S_1S_2S_2$ and symbols $-S_2^*-S_2^*S_1^*S_1^*$ are not a shifted version of a single code sequence required by claim 39. Thus, the symbols from transformer 88 are not a first shift of a code sequence and a second shift of the code sequence as required by claim 39. Examiner cites col. 5, lines 12-16 of Whinnett et al. to justify the interpretation that something is a code sequence. (Office Action 2/13/2008, page 2). Therein, Whinnett et al. disclose "data source 20 provides a data stream of symbols which may be encoded and interleaved." However, Whinnett et al. offer no details of the encoding process. Thus, any code applied to the symbols does not anticipate a first shift of a code sequence and a second shift of the code sequence as required by claim 39. For the same reason, the encoded symbols themselves cannot be a first shift of a code sequence and a second shift of the code sequence as required by claim 39.

Finally, claim 39 recites "the encoder circuit producing the plurality of symbols and **a sequence of predetermined signals at a first and a second output terminal, wherein the sequence of predetermined signals comprises a code sequence**, and wherein a first shift of the code sequence corresponds to the first output terminal and a second shift of the code sequence corresponds to the second output terminal." (emphasis added). Examiner never indicates where the sequence of predetermined signals of claim 39 might be disclosed by Whinnett et al. In a subsequent rejection of claim 28, however, Examiner states "Fig. 5, 92 adds predetermined signals." (Office Action 2/13/2008, page 3). Here, however, spreaders 92 use exactly the same Walsh code for both upper and lower branches. (col. 5, lines 40-43). Whinnett et al. never disclose that predetermined signals are a first shift of a code sequence and a second shift of the code sequence as required by claim 39. For all the foregoing reasons, therefore, claim 39 is patentable under 35 U.S.C. § 102(e) over Whinnett et al.

B. Claims 28, 30-31, 35, 40-41, 44-45, and 49 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Whinnett et al. (U.S. Pat. No. 6,317,411) in view of Secord et al. (U.S. Pat. No. 6,373,831).

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (MPEP § 2143). Appellants respectfully submit that examiner has failed to meet these criteria. Moreover, the examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the Examiner does not produce a *prima facie* case, the Appellants are under no obligation to submit evidence of nonobviousness. "[t]he key to supporting any rejection under 35 USC 103 is a clear articulation of the reason(s) why the claimed invention would have been obvious." *KSR International Co. v. Teleflex Inc.*, 550 U.S. ___, ___, 82 USPQ2d 1385, 1396 (2007). Moreover, "[r]ejections on obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, 441 F.3d 997, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006). Finally, "[t]he references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention." *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986). Examiner has failed to establish a *prima facie* case of obviousness. Thus, claims 28, 30-31, 35, 40-41, 44-45, and 49 are patentable under 35 U.S.C. § 103(a) over Whinnett et al. in view of Secord et al.

1. SUGGESTION OR MOTIVATION TO COMBINE REFERENCES

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so. *In re Kahn*, 441 F.3d 977, 986, 78 USPQ2d 1329, 1335 (Fed. Cir. 2006) (discussing rationale underlying the motivation-suggestion-teaching test as a guard against using hindsight in an obviousness analysis). "A statement that modifications of the prior art to meet the claimed invention would have been 'well within the ordinary skill of the art at the time the claimed invention was made' because the references relied upon teach that all aspects of the

claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references. *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993). "[R]ejections on obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR*, 550 U.S. at ___, 82 USPQ2d at 1396 quoting *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006). (MPEP § 2143.01).

Here, Examiner offers no rational reason why one of ordinary skill in the art at the time of the present invention would think to combine the transmit diversity scheme of Whinnett et al. with the power control scheme of Secord et al. to produce the present invention. Examiner states "[i]t would have been obvious to one skilled in the art at the time the invention was made to decide whether to transform or not plurality [sic] of symbols at the output terminal to provide additional time diversity." (Office Action of 2/13/2008, page 4). Appellants respectfully disagree. Assuming *arguendo* that diversity is beneficial, Examiner fails to offer any reason why would one of ordinary skill in the art think to disable it apart from improper hindsight in view of the instant specification. Moreover, Examiner fails to offer any reason why would one of ordinary skill in the art of transmit diversity think to look to power control to modify or disable transmit diversity. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985). (MPEP § 2142). Examiner has failed to establish a *prima facie* case of obviousness. Thus, claims 28 and 40 and their respective depending claims are patentable under 35 U.S.C. § 103(a) over the cited references.

2. REASONABLE EXPECTATION OF SUCCESS

A *prima facie* obviousness case requires a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Here, a combination of Whinnett et

al. with Secord et al. offers no chance of success. Examiner states "Whinnett does not teach that circuit [sic] is coupled to receive a control signal, the encoder circuit producing the plurality of symbols at an output terminal and not producing the transform of the plurality of symbols at the output terminal in response to a second value of the control signal. Secord teaches the circuit is coupled to receive a control signal, the encoder circuit producing the plurality of symbols at an output terminal and not producing the transform of the plurality of symbols at the output terminal in response to a second value of the control signal [Col 5, lines 43-49, power control bits which transforms [sic] the signal are only inserted depending on an output signal of MUX 40 in Fig. 5]." (Office Action 2/13/2008, pages 3-4).

Examiner errs in misstating the claim language. Claim 28 recites "the encoder circuit coupled to receive a control signal, the encoder circuit **producing the plurality of symbols at the first output terminal and the transform of the plurality of symbols at the second output terminal in response to a first value of the control signal**, the encoder circuit **producing the plurality of symbols at the first output terminal and not producing the transform of the plurality of symbols at the second output terminal in response to a second value of the control signal.**" Claim 40 recites "the encoder circuit **producing the plurality of first symbols at the first output terminal and the transform of the plurality of first symbols at the second output terminal in response to a first value of the control signal**, the encoder circuit **producing the plurality of first symbols at the first output terminal and not producing the transform of the plurality of first symbols at the second output terminal in response to a second value of the control signal.**" (emphasis added). The correct versions of claims 28 and 40, therefore, require that the encoder circuit produce the plurality of symbols (claim 28) or the plurality of first symbols (claim 40) at the first output terminal for either first or second values of the control signal. The encoder circuit, however, selectively produces a transform of the plurality of symbols (claim 28) or a transform of the first plurality of symbols (claim 40) in response to the value of the control signal.

Examiner apparently misunderstands the disclosure of Secord et al. for several reasons. Referring to Figure 5, Secord et al. state "[t]he power control symbols may be multiplexed onto

the data stream by puncturing out the encoded data bits. The power control symbols are then sent on any or all of the carriers with the user data." (col. 5, lines 43-46). First, Secord et al. fail to teach or suggest that one power control symbol is a transform of another power control symbol. Second, there is no teaching or suggestion as to how or why these power control symbols might be combined with the diversity encoder of Whinnett et al. to produce the present invention apart from Examiner's improper hindsight. Third, Secord et al. teach an advantage to "hopping" the power control symbols to different channels at different times. (col. 5, lines 46-49). This scheme, however, would not work with Whinnett et al. to produce the present invention, since data symbols are produced at the first output terminal for either value of the control signal. Finally, the Honorable Board will appreciate that there is no teaching or suggestion by Examiner or either reference as to how or why MUX 40 of Secord et al. might be combined with the encoder of Whinnett et al. to produce a functional circuit of any kind. They are simply incompatible. Thus, claims 28 and 40 and their respective depending claims are patentable under 35 U.S.C. § 103(a) over the cited references.

3. ALL CLAIM LIMITATIONS

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). If an independent claim is nonobvious under 35 U.S.C. § 103(a), then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). (MPEP § 2143.03).

Claim 28 recites "the encoder circuit coupled to receive a control signal, the encoder circuit **producing the plurality of symbols at the first output terminal and the transform of the plurality of symbols at the second output terminal in response to a first value of the control signal**, the encoder circuit **producing the plurality of symbols at the first output terminal and not producing the transform of the plurality of symbols at the second output terminal in response to a second value of the control signal.**" Claim 40 recites "the encoder

circuit **producing the plurality of first symbols at the first output terminal and the transform of the plurality of first symbols at the second output terminal in response to a first value of the control signal**, the encoder circuit **producing the plurality of first symbols at the first output terminal and not producing the transform of the plurality of first symbols at the second output terminal in response to a second value of the control signal.**" (emphasis added). These features of the claimed invention are described in detail at page 5, line 15 through page 6, line 9.

The foregoing emphasized limitations are not disclosed by any combination of Whinnett et al. and Secord et al. Thus, claims 28 and 40 and their respective depending claims are patentable under 35 U.S.C. § 103(a).

Regarding claims 30 and 44, Examiner alleges "Secord further teaches a diversity control circuit coupled to receive a first input signal, the diversity control circuit producing the control signal corresponding to the first input signal [Col. 5, lines 39-43, MUX 40 in Fig. 5 produces the control signal corresponding to the first input signal from 20]." Examiner misunderstands the disclosure of Secord et al. Circuit 20 produces interleaved data. MUX 30 combines appropriate power control symbols with this interleaved data. The combined data and power control symbols are then sent by MUX 40 to the appropriate user channel. The disclosure of Secord et al. fails to meet the limitations of the control signal or the diversity control circuit of claims 30 and 44.

Regarding claims 31 and 45, Examiner states "Secord further teaches the first input signal corresponds to a Doppler frequency [Col. 5, lines 46-49]." The Honorable Board will find no reference to a Doppler frequency at col. 5, lines 46-49 of Secord et al.

Regarding claims 35 and 49, Examiner states "Whinnett teaches the sequence of predetermined signals comprises a code sequence [Col. 5, lines 12-16], and wherein a first shift of the code sequence corresponds to a first output terminal and a second shift of the coed sequence corresponds to the second output terminal [Col. 5, lines 28-35]. As previously discussed, it is not

clear what Examiner has identified as a code sequence. At any rate, Whinnett et al. do not disclose any details of a code sequence.

Appellants believe it is worth repeating from the KSR Court "[t]he key to supporting any rejection under 35 USC 103 is a clear articulation of the reason(s) why the claimed invention would have been obvious." *KSR International Co. v. Teleflex Inc.*, 550 U.S. ___, ___, 82 USPQ2d 1385, 1396 (2007). Appellants find very little of the present rejection qualifies as a clear articulation. For all the foregoing reasons, therefore, Appellants respectfully request that the Honorable Board find for Appellants and direct allowance of claims 28, 30-35, 39-42, and 44-49.

8. CLAIMS APPENDIX A

Claims 1-27 (Cancelled)

28. (Previously amended) A circuit, comprising

an encoder circuit coupled to receive a plurality of symbols, the encoder circuit producing the plurality of symbols at a first output terminal and a transform of the plurality of symbols at a second output terminal within a time slot, the encoder circuit producing a sequence of predetermined signals interposed with the plurality of symbols, the encoder circuit coupled to receive a control signal, the encoder circuit producing the plurality of symbols at the first output terminal and the transform of the plurality of symbols at the second output terminal in response to a first value of the control signal, the encoder circuit producing the plurality of symbols at the first output terminal and not producing the transform of the plurality of symbols at the second output terminal in response to a second value of the control signal.

29. (Cancelled)

30. (Previously amended) A circuit as in claim 28, further comprising a diversity control circuit coupled to receive a first input signal, the diversity control circuit producing the control signal corresponding to the first input signal.

31. (Previously amended) A circuit as in claim 30, wherein the first input signal corresponds to a Doppler frequency.

32. (Previously amended) A circuit as in claim 31, wherein the diversity control circuit is further coupled to receive a second input signal corresponding to a handoff signal.

33. (Previously amended) A circuit as in claim 30, wherein the first input signal corresponds to a handoff signal.

34. (Previously amended) A circuit as in claim 28, wherein the encoder circuit produces a midamble of the predetermined signals interposed with the plurality of symbols.

35. (Original) A circuit as in claim 28, wherein the sequence of predetermined signals comprises a code sequence, and wherein a first shift of the code sequence corresponds to the first output terminal and a second shift of the code sequence corresponds to the second output terminal.

Claims 36-38 (Cancelled)

39. (Original) A circuit, comprising an encoder circuit coupled to receive a plurality of symbols, the encoder circuit producing the plurality of symbols and a sequence of predetermined signals at a first and a second output terminal, wherein the sequence of predetermined signals comprises a code sequence, and wherein a first shift of the code sequence corresponds to the first output terminal and a second shift of the code sequence corresponds to the second output terminal.

40. (Previously amended) A circuit, comprising:

an encoder circuit coupled to receive a plurality of first symbols corresponding to a first user, the encoder circuit producing the plurality of first symbols at a first output terminal and a transform of the plurality of first symbols at a second output terminal within a time slot, the encoder circuit coupled to receive a control signal, the encoder circuit producing the plurality of first symbols at the first output terminal and the transform of the plurality of first symbols at the second output terminal in response to a first value of the control signal, the encoder circuit producing the plurality of first symbols at the first output terminal and not producing the transform of the plurality of first symbols at the second output terminal in response to a second value of the control signal;

a first multiplier circuit coupled to receive the plurality of first symbols and arranged to multiply the plurality of first symbols by a code corresponding to the first user to produce a first coded signal, wherein the first coded signal is applied to a first antenna; and

a second multiplier circuit coupled to receive the transform of the plurality of first symbols and arranged to multiply the transform of the plurality of first symbols by the code corresponding to

the first user to produce a second coded signal, wherein the second coded signal is applied to a second antenna.

41. (Previously added) A circuit as in claim 40, comprising a third multiplier circuit coupled to receive a plurality of second symbols and arranged to multiply the plurality of second symbols by a code corresponding to a second user to produce a third coded signal.

42. (Previously added) A circuit as in claim 41, wherein the third coded signal is applied to the first antenna and not the second antenna.

43. (Cancelled)

44. (Previously amended) A circuit as in claim 40, comprising a diversity control circuit coupled to receive a first input signal, the diversity control circuit producing the control signal corresponding to the first input signal.

45. (Previously added) A circuit as in claim 44, wherein the first input signal corresponds to a Doppler frequency.

46. (Previously added) A circuit as in claim 45, wherein the diversity control circuit is further coupled to receive a second input signal corresponding to a handoff signal.

47. (Previously added) A circuit as in claim 44, wherein the first input signal corresponds to a handoff signal.

48. (Previously added) A circuit as in claim 40, wherein the encoder circuit produces a midamble of predetermined signals interposed with the plurality of first symbols.

49. (Previously added) A circuit as in claim 48, wherein the predetermined signals comprise a code sequence, and wherein a first shift of the code sequence corresponds to the first output terminal and a second shift of the code sequence corresponds to the second output terminal.

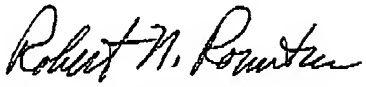
9. EVIDENCE APPENDIX

None.

10. RELATED PROCEEDINGS APPENDIX

None.

Respectfully submitted,



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